IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Takashi OHSUMI

Attn: Applications Branch

Divisional of Serial No.: 09/580,624

Attorney Docket No. IIZ.003D2

Filed: May 30, 2000

For: SEMICONDUCTOR APPARATUS HAVING AN INSULATING LAYER OF VARYING HEIGHT THEREIN

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Preliminary to the examination of the above-identified application, please enter the following amendments and remarks.

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/580,624 which has been allowed, which is a divisional of Serial No. 08/959,667, now U.S. Patent No. 6,097,091, which is hereby incorporated by reference in its entirety for all purposes.--

IN THE CLAIMS

Please cancel claims 1-20 without prejudice.

Please amend the following claim:

21. (Amended) A method for fabricating a semiconductor apparatus, comprising:

fabricating a semiconductor substrate which comprises a semiconductor integrated circuit, and an electrode, which is composed of a base member of insulating material formed on the semiconductor integrated circuit and a conductive layer formed on the surface of the base member;

placing the semiconductor substrate to face a connection substrate;

connecting the electrode to the connection substrate; and

supplying a seal member in the space between the semiconductor substrate and the connection substrate.

Please add the following claims:

--22. A method according to claim 21, wherein

the semiconductor substrate is placed to face the connection substrate according to a face down technique.

23. A method according to claim 21, wherein

the base member and the seal member are made of the same material.--

REMARKS

By this Preliminary Amendment, the specification has been revised to identify the parent application, and claims 1-20 have been canceled. Claim 22-23 have added. Entry of this Preliminary Amendment is respectfully requested.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Susan S. Morse (Reg. No. 35,292) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any over payment to Deposit Account No. 50-0238 for any additional fee required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

JONES VOLENTINE, P.L.L.C.

By: [signature]
Susan S. Morse
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Date: August 3, 2001

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21. (Amended) A method for fabricating a semiconductor apparatus, comprising [the steps of]:

fabricating a semiconductor substrate which comprises a semiconductor integrated circuit, and an electrode, which is composed of a base member of insulating material formed on the semiconductor integrated circuit and a conductive layer formed on the surface of the base member;

placing the semiconductor substrate to face a connection substrate [according to a face-down technique];

connecting the electrode to the connection substrate; and

[filling] supplying a seal member in the space between the semiconductor substrate and the connection substrate[, wherein

the base member and the seal member are made of the same material].